Amendments to the Specification:

Please replace the paragraph beginning on page 2, line 2 with the following amended paragraph:

In one aspect, a transformation engine includes an address generator; a butterfly unit coupled to the address generator; a twiddle LUT coupled to the address generator; and a ~~multiplexer~~ multiplier having a first input coupled to the butterfly unit and a second input coupled to the twiddle LUT.

Please replace the paragraph beginning on page 2, line 6 with the following amended paragraph:

Implementations of the above system may include one or more of the following. The butterfly unit can compute fast fourier transform (FFT) operations. The butterfly unit can compute decimation in frequency fast fourier transform (DIF FFT) operations. The butterfly unit can also compute fast Hadamard transform (FHT) operations. The twiddle LUT contains twiddle factors set to one. Input data belonging to FHT samples are mapped to predetermined inputs. Remaining input data is set to zero. An input buffer can be coupled to the butterfly unit. An output buffer can be coupled to the ~~multiplexer~~ multiplier.

Please replace the paragraph beginning on page 7, line 7 with the following amended paragraph:
FIG. 3 shows an exemplary 64-point Radix 4, Decimation in Frequency FFT structure with 64 inputs and 64 output. FIG. 4 shows the application of the 64-point Radix-4 FFT structure of FIG. 3 in computing a Fast Hadamard transform for input vector length 8 of FIG. 2. The mapping between the FFT input ports and the FHT input signals is given in Table 1. The dashed lines in ~~gray~~ FIG. 4 indicate the data flow for FHT. It can be seen from the figures that four of the FFT butterflies are re-used in the first stage, 8 of them in the second stage and 16 of them in the third stage. FIG. 5 shows an exemplary butterfly re-use pattern for re-using the Radix-4 DIF FFT engine for the computation of FHT. The circles represent the butterflies and the dark circles are re-used.

Please replace the paragraph beginning on page 7, line 16 with the following amended paragraph:

FIG. 6 shows the exemplary engine 30 that can be programmably selected as an FFT engine or an FHT engine. The engine 30 has an input buffer 32 that receives data to be processed. The input buffer 32 is driven by an address generator 34. The output of the input buffer 32 is received by a butterfly unit 36. The output of the butterfly unit 36 is provided to a P/S unit 38. The address generator 34 also drives the P/S unit 38. The output of the P/S unit 38 is provided to one input of a complex multiplier 40, while a second input of the complex multiplier 40 receives the output of a twiddle LUT 42. The address generator 34 also drives the address input of the twiddle LUT 42. The output of the ~~multiplexer~~ multiplier is saved in an output buffer 44 whose address input is driven by the address generator 34. The output of the output buffer 44 is presented to the channel decoder 70.

Please replace the paragraph beginning on page 12, line 3 with the following amended paragraph:

A transformation engine includes an address generator; a butterfly unit coupled to the address generator; a twiddle LUT coupled to the address generator; and a ~~multiplexer~~ multiplier having a first input coupled to the butterfly unit and a second input coupled to the twiddle LUT.